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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/714,935	MAEDA ET AL.	
	Examiner	Art Unit	
	JIMMY H. NGUYEN	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 February 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,8-18,20-25 and 29-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,8-18,20-25 and 29-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/19/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is made in response to applicant's amendment filed on 02/12/2009. Claims 1-3, 8-18, 20-25 and 29-33 are currently pending in the application. An action follows below:

Claim Objections

2. Claims 21-25 are objected to because of the following informalities: "the unit circuits for the first shift register" in line 2 should be changed to -- the **first** unit circuits for the first shift register", so as to make the feature of this claim consistent with the feature in lines 2-3 of independent claim 1. Appropriate correction is required.

3. Claim 33 is objected to because of the following informalities: "the first **unit** circuit" in line 9 should be changed to -- the first circuit --, so as to make the feature of this claim consistent with the feature in line 2 (see any of claims 29-32, e.g., line 18 of claim 32). Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 2 and 18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As to claim 2, this claim recites a feature, "**the** unit circuits" in line 2. Since it is unclear that "the unit circuits" are referred to "first unit circuits" in line 3, "second unit circuit" in line 10, or both, it is considered that the invention is not clearly defined.

Claim 18 recites the limitation "**the** other circuits" in line 2. There is insufficient antecedent basis for this limitation in the claim.

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claims 3 and 29-33 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

As to **claim 3**, this claim (when being read together with independent claim 1) recites limitations, "**the first circuit is a second unit circuit** for a second shift register different from the first shift register" presently recited in lines 10-11 of claim 1 and "the first circuit includes a processing circuit uses output of one of the **first** unit circuits" presently recited in lines 3-4 of claim 3. In other words, this claim requires "the first circuit, which is a **second** unit circuit for a second shift register, includes a processing circuit uses output of one of the **first** unit circuits", which was not supported in the original disclosure.

As best understood, the original disclosure, e.g., Fig. 14, explicitly teaches a second unit circuit (**F/F2**; Fig. 14; page 4, lines 11-12) for a second shift register (SR2) and a processing circuit (**WR2**) using output of one of the **second** unit circuits (F/F2). In other words, the original disclosure does not teach "the first circuit, which is a **second** unit circuit for a second shift

register, includes a processing circuit uses output of one of the **first** unit circuits", as presently claimed.

Further, note that the original disclosure explicitly defines a flip-flop (F/F1 or F/F2), as a unit circuit (see the specification, page 4, lines 11-12), which does not include a processing circuit (WR1 or WR2) (see Fig. 14).

Accordingly, this claim recites the above underlined limitations, which were not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

As to **new claims 29-33**, these claims recite a limitation, "the first circuit is a processing circuit which uses output of one of the first unit circuits, a second unit circuit for a second shift register different from the first shift register, and a processing circuit which uses output of the second unit circuit of the second shift register" in lines 10-13 of claim 29, lines 11-14 of claim 30, lines 12-15 of claim 31, lines 17-20 of claim 32, and lines 9-12 of claim 33. Note that the above underlined limitation includes the following features:

(i) "the first circuit is a processing circuit which uses output of one of the first unit circuits";

(ii) "the first circuit is a processing circuit which uses output of a second unit circuit for a second shift register different from the first shift register"; and

(iii) "**the first circuit is a processing circuit which uses output of a processing circuit which uses output of the second unit circuit of the second shift register**."

The original disclosure, specifically Fig. 14, discloses the above features (i) and (ii), but does not explicitly teach the feature (iii), "**the first circuit is a processing circuit which uses output of a processing circuit which uses output of the second unit circuit of the second shift register**."

Accordingly, these claims recite the above underlined limitation, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1, 2, 8-10, 13-18, 20-25, and 29-33 are rejected under 35 U.S.C. 102(b) as being anticipated by Kihara et al. (US 5,889,504), hereinafter Kihara.

As to claims 1, 8, 9, 13, 17 and 20-25, Kihara discloses **a display device** (an active matrix LCD; see Fig. 2) comprising:

a plurality of data signal lines (data lines D1, D2,...; Fig. 2; col. 4, line 29);

a plurality of scanning signal lines (scanning lines G1, G2,...; Fig. 2; col. 4, lines 26-27) intersecting with the data signal lines (Fig. 2);

pixels (pixel cells GC; Fig. 2; col. 4, line 42) provided for each pair of the data signal lines and the scanning signal lines (Fig. 2);

a scanning signal line driving circuit (a gate driver 2; Fig. 2) for driving the scanning signal lines; and

a data signal line driving circuit (a data driver 3; Fig. 2) comprising **a sampling section** (a sampling transistor circuit 4; Fig. 2) for driving a plurality of data signal lines (D1, D2,...) by sampling image data from an image signal according to a selection signal (Fig. 2; col. 5, lines 29-44) sequentially outputted from a shift register block (a shift register circuit 5; Fig. 2), so as to transfer the image data to the data signal lines (col. 5, lines 29-44), and **a shift register block** (a shift register circuit 5; Fig. 2).

Kihara further teaches the **shift register block** (a shift register circuit 5; Fig. 3) comprising:

a system of a **first shift register** (a system including left-shifting normal registers SR1 of the shift register groups 11 of the 1st-system shift register blocks; best seen in Figs. 5A-5B, 6) comprising a plurality of cascade-connected first unit circuits (left-shifting normal registers SR1 of the first shift register groups 11; Figs. 5A-5B, 6) for sequentially propagating a first input signal therethrough in response to a first clock signal (CK1) (Fig. 8; col. 5, line 57 through col. 6, line 23); and

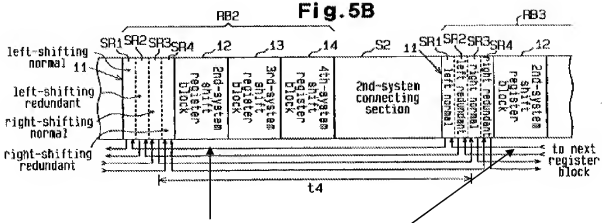
a system of a **second shift register** (a system including left-shifting normal registers SR1 of the second shift register groups 12 of the 2nd-system shift register blocks; best seen in Figs. 5A-5B, 6) comprising a plurality of cascade-connected second unit circuits (left-shifting normal registers SR1 of the second shift register groups 12; see Figs. 5A-5B, 6) for sequentially

propagating a second input signal therethrough in response to a second clock signal (CK2) (Fig. 8; col. 5, line 57 through col. 6, line 23); wherein the second unit circuits (SR1 of the second register groups 12), as also being the claimed first circuits, are linearly aligned with the first unit circuits (SR1 of the first register groups 11) and the second unit circuits (SR1 of the second register groups 12) are disposed in physical spaces between the first unit circuits (SR1 of the first register groups 11) (see Figs. 4-6).

Regarding to the limitation, "signal paths for the first and second shift registers are provided separately for each of the first and second shift registers on respective sides of a circuit alignment of the first and second unit circuits of the first and second shift registers" (see lines 12-14 of claim 1), Kihara discloses that the signal paths (the paths connecting the left-shifting normal register SR1 to the next left-shifting normal register of the first shift register groups 11; see the below annotated Fig. 5B) for the first shift registers (left-shifting normal registers SR1 of the first shift register groups 11; Figs. 5A-5B, 6) are provided on the **bottom** of the circuit alignment of the unit circuits of the first and second shift registers (Fig. 5A, 5B) and the (output) signal paths for the second shift registers (left-shifting normal registers SR1 of the second shift register groups 12; see the below annotated Fig. 6) are provided on the **top** of a circuit alignment of the unit circuits of the first and second shift registers (see the below annotated Fig. 6).

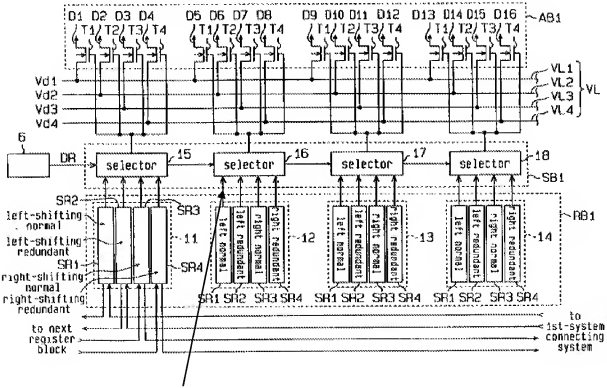
Accordingly, all limitations of these claims are read in the Kihara reference.

Fig.5B



signal paths for the first shift register

Fig.6



one of the signal paths for the second shift register

As to claim 2, Kihara discloses the first unit circuits (left-shifting normal registers SR1 of the first shift register groups 11; Figs. 5A-5B, 6), each comprising a flipflop circuit constituted by inverter circuits (90-92) (Fig. 8).

As to claim 10, Kihara discloses the sampling section (4) simultaneously carrying out sampling of image data of divided image signals which are generated by dividing the image signal according to an alignment order of the data signal lines (col. 5, lines 29-44).

As to claims 14-15, Kihara teaches the data signal line driving circuit 3) and the scanning signal line driving circuit (2) formed on a substrate on which the pixels are formed (see Fig. 2; col. 4, lines 21-25); the pixels, the data signal line driving circuit, and the scanning signal line driving circuit including active elements (TFTs), respectively, each of which is made of a polysilicon thin film transistor (see col. 10, line 62 through col. 11, line 15).

As to claim 16, Kihara teaches the active elements formed on a glass substrate at a process temperature of about 550°C, i.e., not more than 600°C (see at least col. 12, line 58 through col. 13, line 3).

As to claim 18, as discussed in the rejection to claim 17 above, Kihara teaches the other circuits or the second unit circuits (left-shifting normal registers SR1 of the second shift register groups 12; Figs. 5A-5B, 6) comprising circuits (Fig. 8), each including elements 90-92 and their connections and corresponding each of the claimed waveform processing circuits.

As to claims 29-33, Kihara discloses **a display device** (an active matrix LCD; see Fig. 2) comprising:

a plurality of data signal lines (data lines D1, D2,...; Fig. 2; col. 4, line 29);

a plurality of scanning signal lines (scanning lines G1, G2,...; Fig. 2; col. 4, lines 26-27) intersecting with the data signal lines (Fig. 2);

pixels (pixel cells GC; Fig. 2; col. 4, line 42) provided for each pair of the data signal lines and the scanning signal lines (Fig. 2);

a scanning signal line driving circuit (a gate driver 2; Fig. 2) for driving the scanning signal lines; and

a data signal line driving circuit (a data driver 3; Fig. 2) comprising **a sampling section** (a sampling transistor circuit 4; Fig. 2) for driving a plurality of data signal lines (D1, D2,...) by sampling image data from an image signal according to a selection signal (Fig. 2; col. 5, lines 29-44) sequentially outputted from a shift register block (a shift register circuit 5; Fig. 2), so as to transfer the image data to the data signal lines (col. 5, lines 29-44), and **a shift register block** (a shift register circuit 5; Fig. 2).

Kihara further teaches the **shift register block** (a shift register circuit 5; Fig. 3) comprising:

a system of a **first shift register** (a system including left-shifting normal registers SR1 of the shift register groups 11 of the 1st-system shift register blocks; best seen in Figs. 5A-5B, 6) comprising a plurality of cascade-connected first unit circuits (left-shifting normal registers SR1 of the first shift register groups 11; Figs. 5A-5B, 6) for sequentially propagating a first input signal therethrough in response to a first clock signal (CK1) (Fig. 8; col. 5, line 57 through col. 6, line 23); and

a system of a **second shift register** (a system including left-shifting normal registers SR1 of the second shift register groups 12 of the 2nd-system shift register blocks; best seen in Figs.

5A-5B, 6) comprising a plurality of cascade-connected second unit circuits (left-shifting normal registers SR1 of the second shift register groups 12; see Figs. 5A-5B, 6) for sequentially propagating a second input signal therethrough in response to a second clock signal (CK2) (Fig. 8; col. 5, line 57 through col. 6, line 23); wherein the second unit circuits (SR1 of the second register groups 12) are linearly aligned with the first unit circuits (SR1 of the first register groups 11) and the second unit circuits (SR1 of the second register groups 12), as also being the claimed first circuits, are disposed in physical spaces between the first unit circuits (SR1 of the first register groups 11) (see Figs. 4-6).

Regarding to limitation, "the first circuit is a processing circuit which uses output of one of the first unit circuits, a second unit circuit for a second shift register different from the first shift register, and a processing circuit which uses output of the second unit circuit of the second shift register" (see lines 10-13 of claim 29, lines 11-14 of claim 30, lines 12-15 of claim 31, lines 17-20 of claim 32, and lines 9-12 of claim 33), Kihara teaches that the **current** second unit circuit (left-shifting normal registers SR1 of the second shift register groups 12; see Figs. 5A-5B, 6), **as the claimed first circuit** or **the claimed processing circuit**, uses output of the **next right** second unit circuit (the next left-shifting normal registers SR1 of the second shift register groups 12 on the right; see Figs. 5A-5B, 6) for a second shift register different from the first shift register.

Regarding to the limitation, "signal paths for the first and second shift registers are provided separately for each of the first and second shift registers on respective sides of a circuit alignment of the first and second unit circuits of the first and second shift registers" of these claims, see the rejection to claim 1 above.

Accordingly, all limitations of these claims are read in the Kihara reference.

10. Claims 1-3, 8-10, 12-18, 20-25 and 29-33 are rejected under 35 U.S.C. 102(e) as being anticipated by Azami (US 6,702,407 B2).

As to claims 1, 2, 8-10, 13, 17 and 20, Azami discloses **a display device** (an active matrix image display device; see col. 6, line 52 and Fig. 30), comprising:

a plurality of data signal lines (source signal lines 104/SL; see Fig. 30; col. 1, line 35; col. 7, line 37);

a plurality of scanning signal lines (gate signal lines 105; see Fig. 30; col. 1, line 36) intersecting with the data signal lines (104/SL); pixels (Fig. 30, col. 1, line 39) provided for each pair of the data signal lines and the scanning signal lines;

a scanning signal line driving circuit (a gate signal line driving circuit 102; see Fig. 30; col. 1, line 31) for driving the scanning signal lines; and

a data signal line driving circuit (a source signal line driving circuit 101; see Figs. 3 and 30; col. 1, line 30) comprising **a sampling section** (a section including first and second latch portions, P/S conversion circuits, D/A conversion circuit, and a source line selecting circuits; see Fig. 3) for driving a plurality of data signal lines (SL) by sampling image data from an image signal according to a selection signal (output of a FF; see Fig. 3) sequentially outputted from a shift register block (a shift register portion; see Fig. 3), so as to transfer the image data to the data signal lines, and **a shift register block** (a shift register portion).

Azami further teaches the **shift register block** (a shift register portion; see Fig. 3) comprising a **first shift register** (a first shift register comprising, e.g., first 4 flipflop (FF) circuits; see Fig. 3) and a second shift register (a second shift register comprising next 4 FF

circuits and inverters and NAND gates and their connections associated with the first four FF circuits; see Fig. 3).

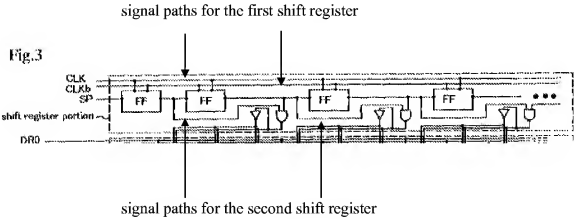
Azami teaches the first shift register comprising **4 first unit circuits** (4 FF circuits) spaced-apart cascade-connected; outputting an input signal (a start pulse SP; see Fig. 3) in response to a clock signal (CLK; see Fig. 3, col. 6, lines 64-67); and sequentially outputting a selection signal from output-stages comprised of the unit circuits (see Fig. 3, col. 6, lines 64-67). Azami further teaches the first unit circuits (FF circuits) of the first shift register being linearly disposed so that physical spaces are provided between adjacent pairs of the unit circuits (see Fig. 3).

Azami further teaches that **first circuits are the second unit circuits, (each circuit including an inverter, an NAND, and their connections**; see Fig. 3), are different from the first unit circuits (first 4 FFs) of the first shift register, are disposed in the physical spaces between adjacent first unit circuits (FFs), and have outputs, which are not supplied to any of the first unit circuits (FF circuits) of the first shift register (see Fig. 3).

Regarding to the limitation, "signal paths for the first and second shift registers are provided separately for each of the first and second shift registers on respective sides of a circuit alignment of the first and second unit circuits of the first and second shift registers" (see lines 12-14 of claim 1), Azami teaches the signal paths for the first shift register (paths for transmitting clock signals to each FF circuit of the first shift register; see the below annotated Fig. 3) provided on the **top side** of a circuit alignment of the unit circuits of the first and second shift registers and the signal paths for the second shift register (paths for transmitting the output signals from the inverters and NAND gates to the first latch portion; see the below annotated Fig. 3) provided on

the **bottom side** of a circuit alignment of the unit circuits of the first and second shift registers (see the below annotated Fig. 3).

Accordingly, all limitations of these claims are read in the Azami reference.



As to claims 3 and 18, as discussed above, each first circuit including an inverter, an NAND, and their connections (see Fig. 3) are considered as a processing circuit (of claim 3) or waveform processing circuit (of claim 18).

As to claim 12, Azami teaches the image signal being digital signal (DR0-DR2, DG0-DG2 and DB0-DB2; see Fig. 3; col. 7, lines 10-14) and the first circuit (a circuit including an inverter, an NAND, and their connections; see Fig. 3) comprising an output circuit, which use outputs of the unit circuits of the first shift register (see Fig. 3).

As to claims 14-15, Azami teaches the data signal line driving circuit and the scanning signal line driving circuit formed on a substrate on which the pixels are formed (see col. 10, lines 33-42); the pixels, the data signal line driving circuit, and the scanning signal line driving circuit

including active elements (TFTs), respectively, each of which is made of a polysilicon thin film transistor (see col. 10, lines 33-42 and col. 15, lines 6-27).

As to claim 16, Azami teaches the active elements formed on a glass substrate at a process temperature of not more than 600°C (see at least at col. 10, line 56 through col. 67; col. 11, lines 39-46; col. 15, lines 21-27).

As to claims 21-25, Azami teaches the unit circuits (first four flip-flop (FF) circuits; Fig. 3), for the first shift register, disposed linearly with the first circuit or the circuits other than the unit circuits of the first shift register (Fig. 3).

As to claims 29-33, Azami discloses **a display device** (an active matrix image display device; see col. 6, line 52 and Fig. 30), comprising:

a plurality of data signal lines (source signal lines 104/SL; see Fig. 30; col. 1, line 35; col. 7, line 37);

a plurality of scanning signal lines (gate signal lines 105; see Fig. 30; col. 1, line 36) intersecting with the data signal lines (104/SL); pixels (Fig. 30, col. 1, line 39) provided for each pair of the data signal lines and the scanning signal lines;

a scanning signal line driving circuit (a gate signal line driving circuit 102; see Fig. 30; col. 1, line 31) for driving the scanning signal lines; and

a data signal line driving circuit (a source signal line driving circuit 101; see Figs. 3 and 30; col. 1, line 30) comprising **a sampling section** (a section including first and second latch portions, P/S conversion circuits, D/A conversion circuit, and a source line selecting circuits; see Fig. 3) for driving a plurality of data signal lines (SL) by sampling image data from an image

signal according to a selection signal (output of a FF; see Fig. 3) sequentially outputted from a shift register block (a shift register portion; see Fig. 3), so as to transfer the image data to the data signal lines, and **a shift register block** (a shift register portion).

Azami further teaches the **shift register block** (a shift register portion; see Fig. 3) comprising a **first shift register** (a first shift register comprising, e.g., first 4 flipflop (FF) circuits; see Fig. 3) and **a second shift register** (a second shift register comprising next 4 FF circuits and inverters and NAND gates and their connections associated with the first four FF circuits; see Fig. 3).

Azami teaches the first shift register comprising **4 first unit circuits** (4 FF circuits) spaced-apart cascade-connected; outputting an input signal (a start pulse SP; see Fig. 3) in response to a clock signal (CLK; see Fig. 3, col. 6, lines 64-67); and sequentially outputting a selection signal from output-stages comprised of the unit circuits (see Fig. 3, col. 6, lines 64-67). Azami further teaches the first unit circuits (FF circuits) of the first shift register being linearly disposed so that physical spaces are provided between adjacent pairs of the unit circuits (see Fig. 3).

Azami further teaches that a first circuit (each circuit including an inverter, an NAND, and their connections; see Fig. 3), which is not one of the first unit circuits of the first shift register, is disposed in the physical space between a first unit circuit of a preceding output stage and a first unit circuit of a following output stage (see Fig. 3).

Azami further teaches the first circuit is a processing circuit which uses output of one of the first unit circuits (Fig. 3).

Regarding to the limitation, "signal paths for the first and second shift registers are provided separately for each of the first and second shift registers on respective sides of a circuit alignment of the first and second unit circuits of the first and second shift registers" (see lines 12-14 of claim 1), see the rejection to claim 1 above.

Accordingly, all limitations of these claims are read in the Azami reference.

11. Claims 1-3, 8-10, 13-18, 20-25 and 29-33 are rejected under 35 U.S.C. 102(e) as being anticipated by Washio et al. (US 6,724,361 B1), hereinafter Washio.

As to claims 1, 2, 8-10, 13, 17, and 20, Washio discloses **a display device** (an image display device **11**; see Fig. 2; col. 10, line 4), comprising **a plurality of data signal lines** (data signal lines SL1-SLn; see Fig. 2; col. 10, line 11); **a plurality of scanning signal lines** (scanning signal lines GL1-GLn; see Fig. 20; col. 10, lines 8-9) intersecting with the data signal lines (SL); pixels (16) (see Fig. 2, col. 10, line 12) provided for each pair of the data signal lines and the scanning signal lines; **a scanning signal line driving circuit** (a gate signal line driving circuit 13; see Fig. 2; col. 10, line 19) for driving the scanning signal lines; and **a data signal line driving circuit** (a data signal line driving circuit 14; see Fig. 2; col. 10, line 29) comprising **a sampling section** (18) (see Fig. 2) for driving a plurality of data signal lines (SL) by sampling image data from an image signal according to a selection signal (output of a FF; see Fig. 3) sequentially outputted from **a shift register block** (a shift register 1/27; see Figs. 2 and 11), so as to transfer the image data to the data signal lines, and a shift register block (1/27) (see col. 10, lines 28-38). Washio further teaches the **shift register block** (27) comprising a **first shift register** (a first shift register comprising, e.g., first 4 flipflops (FFs) 23; see Fig. 11) and **a**

second shift register (a second shift register comprising next 4 FFs 23 and inverters 24 associated with the first four FF circuits; see Fig. 11).

Washio teaches the first shift register comprising **4 first unit circuits** (4 FFs 23) spaced-apart cascade-connected; outputting an input signal (a signal inputted in S terminal of the first FF 23; see Fig. 11) in response to a clock signal (SCK/SCKB; see Fig. 11, col. 12, lines 55-67); and sequentially outputting a selection signal from output-stages comprised of the unit circuits (23) (see Fig. 11, col. 15, line 59 through col. 16, line 21). Washio further teaches the first unit circuits (FFs 23) of the first shift register being linearly disposed so that physical spaces are provided between adjacent pairs of the unit circuits (23) of the first shift register (see Fig. 11). Washio further teaches **first circuit** (each circuit including an inverter 24 and its connections; see Fig. 11) different from the first unit circuits (23) of the first shift register, disposed in the physical spaces between adjacent unit circuits (23), and having outputs, which are not supplied to any of the unit circuits (23) of the first shift register (see Fig. 11). Note that the first circuit (24) is considered as the claimed second unit circuit for the second shift register (a second shift register comprising next 4 FFs 23 and inverters 24 associated with the first four FF circuits; see Fig. 11).

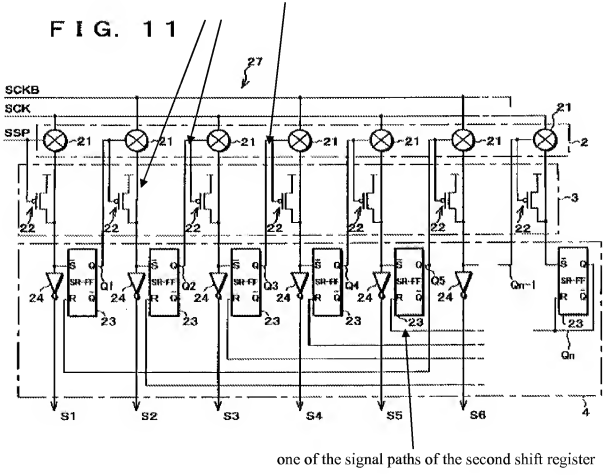
Regarding to the limitation, "signal paths for the first and second shift registers are provided separately for each of the first and second shift registers on respective sides of a circuit alignment of the first and second unit circuits of the first and second shift registers" (see lines 12-14 of claim 1), Washio teaches the **signal paths** for the first shift register (paths for transmitting set signals to Sbar terminals to the first four FFs 23 or output signals Q from the first four FFs 23; see the below annotated Fig. 11) provided on the **top side** of a circuit alignment of the unit

circuits of the first and second shift registers and **signal paths** for the second shift register (paths for transmitting the reset signals R to the R terminal of the next 4 FFs of the second shift register; see the below annotated Fig. 11) provided on the **bottom side** of a circuit alignment of the unit circuits of the first and second shift registers (see the below annotated Fig. 11).

Accordingly, all limitations of these claims are read in the Washio reference.

signal paths of the first shift register

FIG. 11



one of the signal paths of the second shift register

As to claim 3 and 18, as discussed above, the first circuit (24) (e.g., **the second inverter 24** shown in Fig. 11) is considered as a processing circuit (of claim 3) or a waveform processing circuit (of claim 18) (see Fig. 11).

As to claims 14-15, Washio teaches the data signal line driving circuit and the scanning signal line driving circuit formed on a substrate on which the pixels are formed (see col. 38, lines 20-22; col. 41, lines 1-4); the pixels, the data signal line driving circuit, and the scanning signal line driving circuit including active elements (TFTs), respectively, each of which is made of a polysilicon thin film transistor (see col. 17, lines 37-43).

As to claim 16, Washio teaches the active elements formed on a glass substrate at a process temperature of not more than 600°C (see at least at col. 18, lines 31-42; col. 21, lines 27-36; and col. 41, lines 5-9).

As to claims 21-25, Washio teaches the unit circuits (first four flip-flops (FFs) 23; Fig. 11), for the first shift register, disposed linearly with the first circuit or the circuits other than the unit circuits of the first shift register (Fig. 11).

As to claims 29-33, Washio discloses **a display device** (an image display device **11**; see Fig. 2; col. 10, line 4), comprising **a plurality of data signal lines** (data signal lines SL1-SLn; see Fig. 2; col. 10, line 11); **a plurality of scanning signal lines** (scanning signal lines GL1-GLn; see Fig. 20; col. 10, lines 8-9) intersecting with the data signal lines (SL); pixels (16) (see Fig. 2, col. 10, line 12) provided for each pair of the data signal lines and the scanning signal lines; **a scanning signal line driving circuit** (a gate signal line driving circuit 13; see Fig. 2; col. 10, line 19) for driving the scanning signal lines; and **a data signal line driving circuit** (a data

signal line driving circuit 14; see Fig. 2; col. 10, line 29) comprising **a sampling section** (18) (see Fig. 2) for driving a plurality of data signal lines (SL) by sampling image data from an image signal according to a selection signal (output of a FF; see Fig. 3) sequentially outputted from **a shift register block** (a shift register 1/27; see Figs. 2 and 11), so as to transfer the image data to the data signal lines, and a shift register block (1/27) (see col. 10, lines 28-38).

Washio further teaches the **shift register block** (27) comprising a **first shift register** (a first shift register comprising, e.g., first 4 flipflops (FFs) 23; see Fig. 11) and **a second shift register** (a second shift register comprising next 4 FFs 23 and inverters 24 associated with the first four FF circuits; see Fig. 11).

Washio teaches the first shift register comprising **4 first unit circuits** (4 FFs 23) spaced-apart cascade-connected; outputting an input signal (a signal inputted in S terminal of the first FF 23; see Fig. 11) in response to a clock signal (SCK/SCKB; see Fig. 11, col. 12, lines 55-67); and sequentially outputting a selection signal from output-stages comprised of the unit circuits (23) (see Fig. 11, col. 15, line 59 through col. 16, line 21). Washio further teaches the first unit circuits (FFs 23) of the first shift register being linearly disposed so that physical spaces are provided between adjacent pairs of the unit circuits (23) of the first shift register (see Fig. 11). Washio further teaches **first circuit** (each circuit including an inverter 24 and its connections; see Fig. 11) different from the first unit circuits (23) of the first shift register, disposed in the physical spaces between adjacent unit circuits (23), and having outputs, which are not supplied to any of the unit circuits (23) of the first shift register (see Fig. 11).

Washio further teaches that a first circuit (each circuit including an inverter 24 and its connections; see Fig. 11), which is not one of the first unit circuits of the first shift register, is

disposed in the physical space between a first unit circuit of a preceding output stage and a first unit circuit of a following output stage (see Fig. 11).

Washio further teaches the first circuit is a processing circuit which uses output of one of the first unit circuits (Fig. 11).

Regarding to the limitation, "signal paths for the first and second shift registers are provided separately for each of the first and second shift registers on respective sides of a circuit alignment of the first and second unit circuits of the first and second shift registers" (see lines 12-14 of claim 1), see the rejection to claim 1 above.

Accordingly, all limitations of these claims are read in the Washio reference.

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Azami.

As to claim 11, Azami teaches that the circuit (a circuit including an inverter, an NAND, and their connections; see Fig. 3) different from the unit circuits comprises a waveform shaping circuit, a buffer circuit, or a sampling circuit, which uses outputs of the unit circuits (see Fig. 3). Azami further teach the driving system of the source signal line driving circuit including an analog system and a digital system (see col. 1, lines 43-47); therefore, while Azami does not exemplify that the image data being an analog mage data, but it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify the source signal

line driving circuit of Azami to drive an analog image data since the image data can be represented by either one of them and it would not bring any unexpected result.

Response to Arguments

14. Applicant's arguments filed 02/12/2009 have been fully considered but they are not fully persuasive.

Applicant has amended all independent claims to recite limitation, "signal paths for the first and second shift registers are provided separately for each of the first and second shift registers on respective sides of a circuit alignment of the first and second unit circuits of the first and second shift registers" and argued that none of Kihara, Azami, and Washio discloses the underlined limitation. Examiner disagrees and directs the applicant to the above detailed rejections including the annotated drawings to illustrate how the claimed limitation read in these references.

With respect to the rejection under 35 USC 112, first paragraph, to claims 26-28 in the Office Action dated 11/12/2008, this rejection is hereby withdrawn in light of the cancellation to claims 26-28.

Conclusion

15. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jimmy H. Nguyen whose telephone number is 571-272-7675. The examiner can normally be reached on Monday - Friday, 6:30 a.m. - 3:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached at 571-272-7681. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Jimmy H Nguyen/

Primary Examiner, Art Unit 2629